Surface Modifications Used to Create a Universal Approach of Modeling Diodes

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Abstract

To better understand and test current theories of charge transfer across inorganic semiconductor | conjugated polymer interfaces, the work in the Lonergan Labs has shown a correlation between the capacitance-voltage (C-V) and the current-voltage (I-V) characteristics of n-InP | poly (pyrrole) interfaces. Analytical expressions explaining the barrier height have been determined using a novel approach to evaluate the barrier height and model for tunable diodes. The most common anomalies are discrepancies between the interfacial potential barrier heights determined by various techniques. In the past, device behavior is not always reproducible. But, using a thin polyimide film of ~ +3.0 μm can consistently reproduce the past data needed to further expand upon "Moore's Laws." Through this use of chemical surface modifications to control electron transfer at inorganic semiconductor interfaces (IS), a general platform for testing electronic processes at these (IS) interfaces will help to re-engineer conventional microelectronic devices.

Introduction

Developing a pattern upon the face of a substrate (silicon wafer) using polyimide for the construction of a diode has value for sev-

eral reasons. First, once a system for patterning the polyimide film is developed, the procedure is simple and reproducible. Second, once this surface or pattern is developed, the polyimide film is inert to the further chemical reactions involving the manufacture of the diode. Currently the procedure for creating a diode involves the use of Tefzel, an inert material used to define the area on the face of the substrate for a diode. The procedure for patterning is as follows: "Position in metal drilling holder and drill a hole through the cover slip and Tefzel." [Ref #2] This procedure is crude and can result in some uncertainty. One goal is to limit this source of uncertainty.

Statement of purpose

One way to overcome the uncertainty of procedures using Tefzel is to design and develop a diode created by a process that starts with wet chemical etching, a process that will take the place of the procedure involving Tefzel. The first task is to define the area upon a substrate using Wet Etch Polyimide (PI-2545). Using a protocol developed in cooperation with Ben Anger [Ref # 1], this patterning is reproducible and consistent. Next, it is necessary to assemble a diode, as shown in figure1, using a semiconductor with an area of 2mm defined by the polyimide.

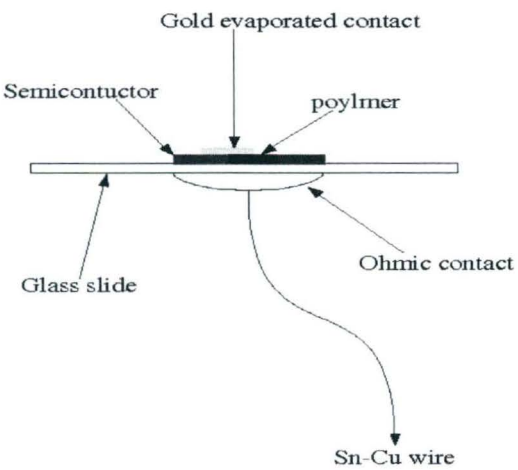


Figure 1, Model of proposed diode.

The long-term goal of the research is to re-engi-

neer the device structure so that we can do the following types of experiments: (i) to understand charge depletion and charge transport at inorganic semiconductor (IS) interfaces; (ii) to evaluate the efficacy of inhomgeneity models in explaining classic anomalies; [Ref # 3] (iii) to understand the potential, limitations, and interpretation of current structure developmental procedures in the re-engineering of nanostructured interfaces.

Well-defined nanostructured interfaces need to be fabricated using wet chemical lithography to define the area for the n-InP / polypyrole interface. Two significant limitations and assumptions are inherent in this research. First, once the area is defined, the polyimide interferes with the electron transfer across the interface. The second limitation focuses on whether it is possible to re-engineer the top contact (gold grid) of the IS interface with a reproducible and controlled procedure.

This work will limit a structural uncertainty while developing a model on a well-defined nanostructure interface. The work, there-

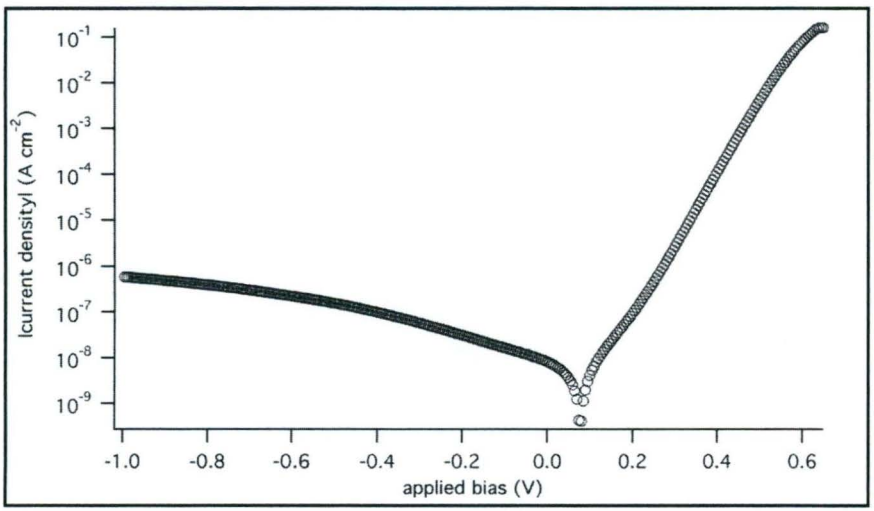


Figure 2, sample current voltage curve.

fore, will test general theories of electron transfer rather than try to control electronic process at the inorganic semiconductor interface due to needed surface modifications [Ref # 3-11].

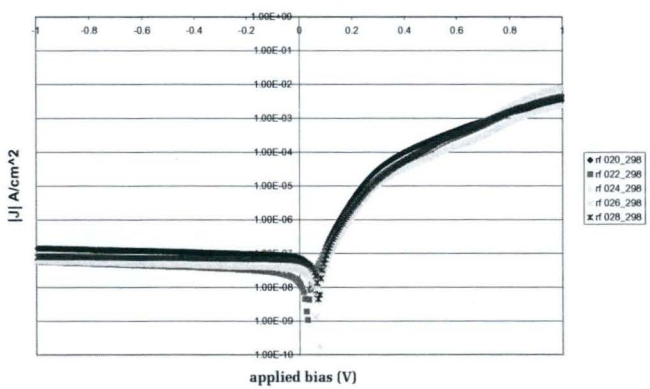
Once the device (IS interface) is engineered and assembled it will be tested by applying a bias (V) to produce an IV curve (current voltage curve) as in fig. 2. This non-symmetric curve shows good current in the positive (+) direction and little current in the negative (-) direction. Thus, the current flow is restricted to one direction as per the definition of a diode [Terminology # 1].

Results

The first diode, rf 020, was completed on June 28, 2004. It was constructed from an n-Si | poly (pyrrole) interface without a poly-imide defined area and using the traditional 4mm tefzel method. The purpose of this procedure was to show that a diode could be constructed with a quality factor consistent with prior data.

These data show that the (I-V) curves for the structures rf 020-28 are consistent with the data for a Schottky diode. Figure 3 shows an absolute current density (|J|)-applied bias (V) plot near room temp (298K) for the diodes rf 020-28.

Figure 3: n-Si | poly(pyrrole) Current Voltage Curves for Diodes rf 020-28



Experiment

The design of the n-InP | poly (pyrrole) diode shown in figure 1 uses a physical mask consisting of Polyimide and a glass cover slip between two layers of Tefzel film, which controls the contact area of the poly (pyrrole) in the semiconductor, A = .0314cm^2.

To complete a poly (imide) conduction test, a thin film (~2.0 μm) must be spin coated on the surface of the semiconductor. This will create the n-InP | poly (imide) interface using the polyimide as a barrier layer between the n-InP and the 4mm gold top contact. The purpose of this test is to show that the polyimide is inert and that there is no electron transfer across the n-InP | poly (imide) interface, as seen in Figure 5.

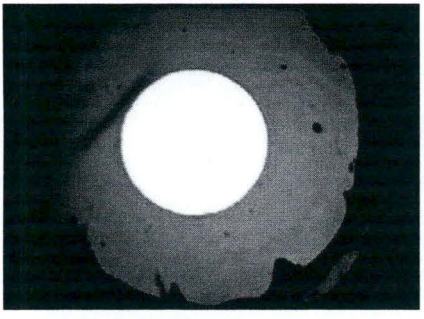


Figure 4: Image showing clear contact area.

An impedance analysis (C-V) of the samples rf 062a shows the polyimide behaves as a capacitor. In figure 6 the plot of the |Z| absolute impedance vs. frequency shows a linear progression in the negative direction as the frequency increases the impedance decreases. As per a log, log plot:

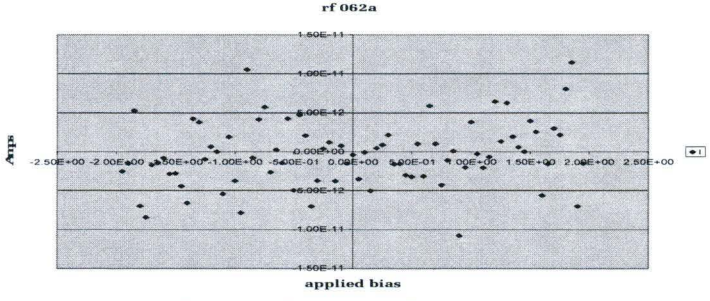


Figure 5: Scatterplot of applied bias.

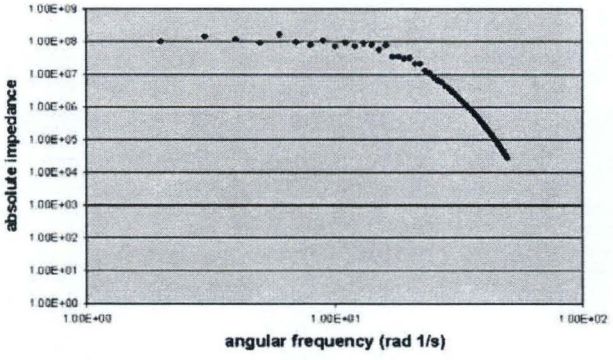


Figure 6: Impedence as a function of angular frequency.

Figure 6 shows that it is possible to extract a value for the slope of the tangent line of |Z| vs. angular frequency. The result, (-1), is consistent with the data for a capacitor.

Impedance analysis (C-V) of the sample rf 062a_298 shows the

$$|Z| = \frac{1}{\omega * c},\ |Z| = (impedance),\ \omega = frequency,$$

$$\log|Z| = \log\left(\frac{1}{\omega * c}\right) \Leftrightarrow \log|Z| = \log\omega^{-1} + \log c^{-1} \Leftrightarrow$$

$$\log|Z| = (-1\log\omega) + (-1\log c).$$

Using $y = mx + b,\ y = \log|Z|,\ b = -1\log c,\ x = \log\omega,\ \forall slope = -1.$

polyimide behaves as a capacitor. In Figure 7, the phase angle of theta vs. frequency = 270 ~ (-90), thus showing that the impedance is strongly capacitive in nature.

Using a poly (imide) film to define the area for the diode as in Figure 1, newly constructed diodes can be used to test established data. With this new surface modification, the uncertainty of past models may be limited leading to a correction of anomalies regarding barrier height extraction.

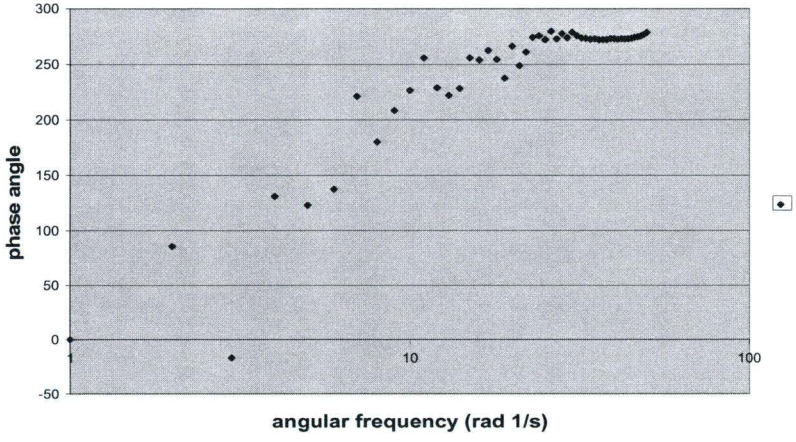


Figure 7: Impedence analysis

Data

Using these n-InP | poly (pyrrole) structures to test current electron transfer theories resulted in two sets of data. First, in figure 8, the data shows the current voltage (I-V) curves for the rf 070b diode

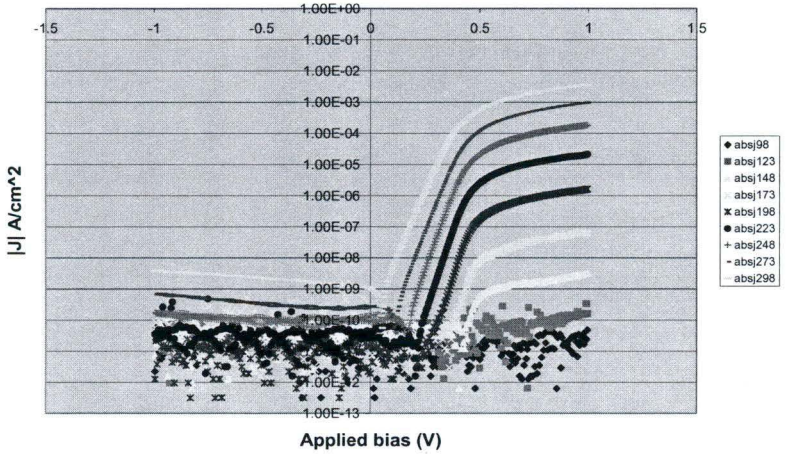


Figure 8: Current Voltage Curves for rf070b Diode

to be consistent with the data from the previous studies of this interface [Ref # 12] and with a good quality factor ~ 1.016435. This data shows that the poly (imide) being used to define the area for the diode is not affecting the current voltage (I-V) measurements for this interface area. The current voltage (I-V) plots extract curves that visually explain the behavior of the diode. These parameters are often voltage independent and are defined within the diode equation:

$$J = J_0 \exp\left(\frac{\beta V_{app}}{n}\right)\left[1 - \exp\left(-\beta V_{app}\right)\right], \quad \text{where} \quad \beta = \frac{q}{kT}$$

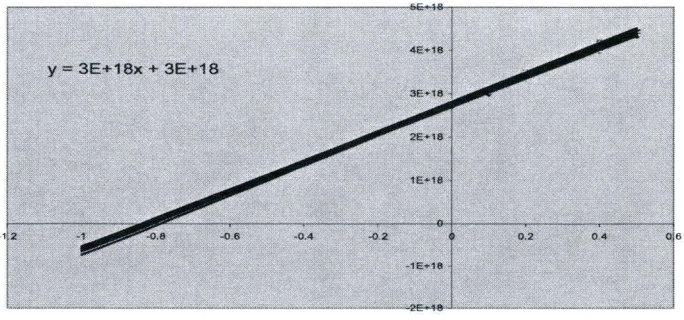
From the (I-V) curve the quality factor is derived from the slope and intercept of the tangent line to the data ln J vs. V_{app} curve (Figure 8). Also, a graph of (capacitance)$^{-2}$ vs. applied bias (V) shows the current storage plots to extract the barrier height (Φb) of the inorganic semiconductor interface.

The second set uses capacitance-voltage (C-V), current storage for rf 070_298 n-InP | poly (pyrrole) structures. To determine the zero-bias barrier height (Φb) of the n-InP | poly (pyrrole) interfaces, tests relied on reverse-biased capacitance measurements and the Mott-Schottky analysis. The data in figure 9 tabulated together calculate, V_I to extract the barrier height given by the equation:

$$\Phi_b = |V_I| + |V_n| + \frac{kT}{q}.$$

V_I represents the equation for the slope of the line extracted by the plot of angular frequency vs. |Z|, absolute impedance and phase angle. This value is the extraction of the value where the trend line = 0 on the x-axis.

Figure 9: 1/C^2 vs. Bias for T298



$$V_n = \frac{kT}{q} * \ln\left(\frac{N_c}{N_d}\right)$$

$$N_c = \frac{1}{4}\left(\frac{2m^* kT}{\Pi(\hbar)^2}\right)^{\frac{3}{2}}$$

$$N_d = \frac{1}{q\mu\rho}$$

$$\rho = \frac{V}{I} * W * CF\Omega cm.$$

From the data extracted in Figure 9, $y = 3E+18x+3E+18$ solving for the variable x exposes the variable for the barrier height calculations. $\because V_I = \sim .841, \frac{-kT}{q} = 0.0254 @ 298K,\ V_n = .0254\ln\left(\frac{N_c}{N_d}\right)$

$$\Rightarrow \frac{1}{4}\left[\left(\frac{2 * 7.015E-32Kg * 1.38E-23\frac{J}{K} * 298K}{\pi\left(\frac{6.63E-34J \bullet s}{\pi}\right)^2}\right)^{\frac{3}{2}}\right]$$

$$N_c = 5.47E+17cm^{-3}$$

$$N_d = 4.6E+15$$

$$V_n = .0254\ln\left(\frac{5.47E+17cm^{-3}}{4.6E+15}\right) \Rightarrow V_n = 0.12707$$

$$\Phi_b = |V_I| + |V_n| + \frac{kT}{q}$$

$\Phi_b = |-0.841| + |0.12707| + 0.0254 \Rightarrow$ The barrier height for rf 070 is 0.96686V, a value inconsistent with the previously determined data for these structures [Ref # 12] and raising a problem. The change in barrier height is problematic of the capacitance generated by the use of the poly (imide). Therefore, there is a need to develop a model to explain this effect. One possible solution uses a dual-parallel capacitor.

Using the model represented in Figure 10, the capacitance of the whole can be calculated by calculating the capacitance of a parallel capacitor.

$$\frac{1}{C_T} = \frac{1}{C_{PP}} + \frac{1}{C_{PI}} \Leftrightarrow C_T = \frac{C_{PP} * C_{PI}}{C_{PP} + C_{PI}} \Leftrightarrow C_T = \left[\left(\frac{C_{PP}}{A_{PP}}\right) + \left(\frac{C_{PI}}{A_{PI}}\right)\right]$$

The results show that by using a thicker poly (imide) film to define the area for the diode, one can increase the impedance of the C_{PI} side of the dual-parallel capacitor, thus reducing the capadance to almost ~ 0, as a function of applied bias (V). This allows the capacitance of the polyimide film creating

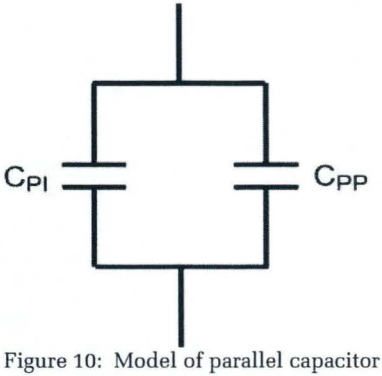


Figure 10: Model of parallel capacitor

the n-InP | poly(pyrrole) interface to be seen as a Mott-Schottky diode.

The plot of the data for rf 080-096 shows a linear trend As the thickness of the polyimide film increases, the barrier height decreases, thus showing that the model proposed in figure 10 holds true for these diodes. The data shows that poly (imide) can be used to define the area for a diode, but the film thickness must be greater than $\sim 3.0 \mu m$, as the diodes rf 080-96a.

Conclusion

The conjugated polymer poly (pyrrole) interfaced to the inorganic semiconductor n-InP with an area of $0.0314\, cm^{-2}$ defined

Figure 11: Barrier height vs. film thickness

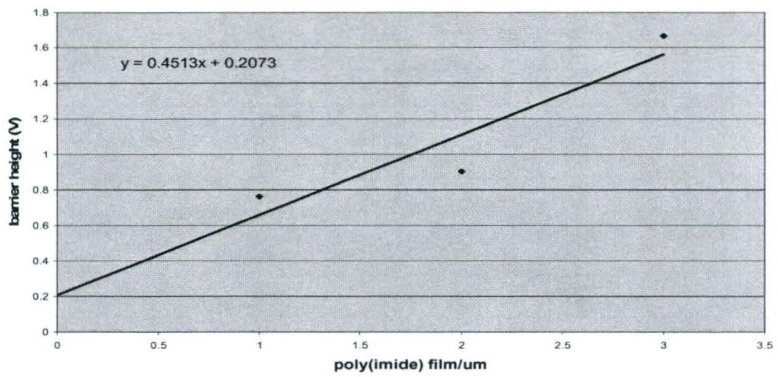


Figure 12: rf 080-096a

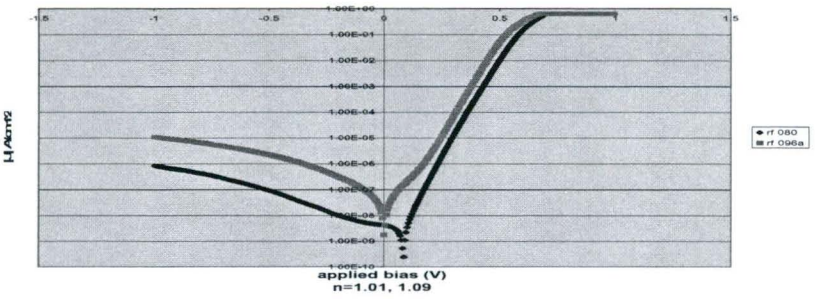
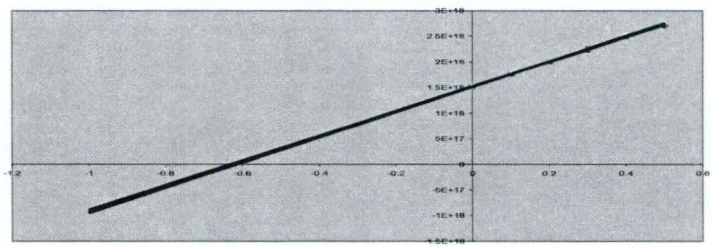


Figure 13: 1/C^2 vs. Bias for T298
Barrier Height = 0.7623 V



by poly (imide) provides a Schottky-type diode with rectification characteristics ($\Phi_b = 0.8eV$ and $n = 1.02$) that compare well with those previously studied n-InP | poly (pyrrole) interfaces [Ref # 12]. This result will allow further surface modifications including the replacement of the gold grid in figure 1 with sputtered gold, which is one aspect of future directions for this research.

Terminology

1. Diode- An electronic device that restricts current flow to one direction.
2. Substrate-The body or base layer of a diode onto which other layers are deposited to form the diode. This substrate is usually silicon.
3. Etching- To cut into the surface of substrate by the action of a chemical reaction.
4. Semiconductor- A material "Substrate", typically crystalline, which allows current to flow under certain circumstances, common semiconductors are silicon and are used to design diodes.
5. IS interfaces- inorganic semiconductors
6. Inhomgeneity- the barrier height is not homogeneous.
7. Anomalies- abnormal
8. Lithography- the chemical transfer of patterns from one surface to another.

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